

Figure 1 Three Transistor Pixel

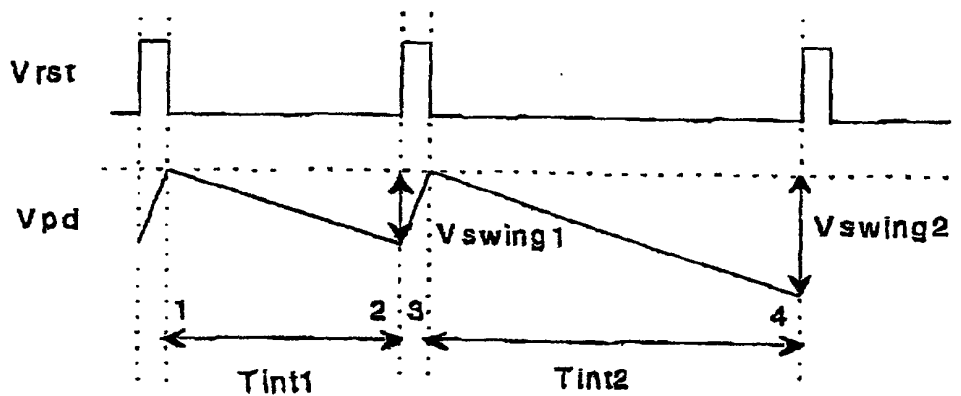


Figure 2 Voltage Swing on Photodiode

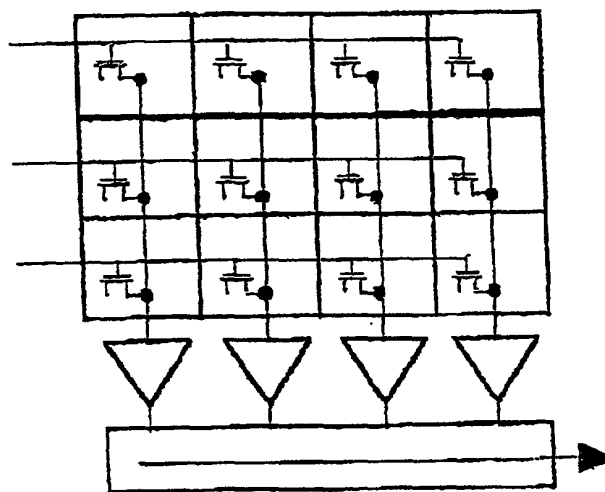


Figure 3 Multiplex Readout

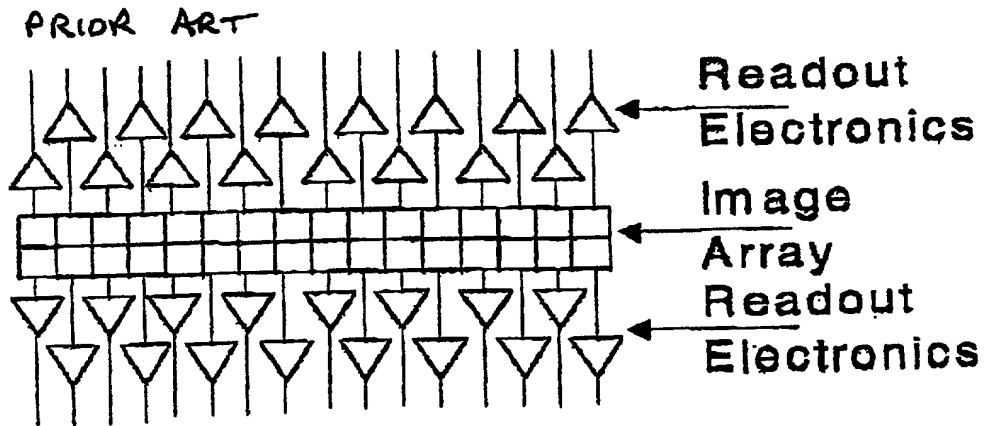
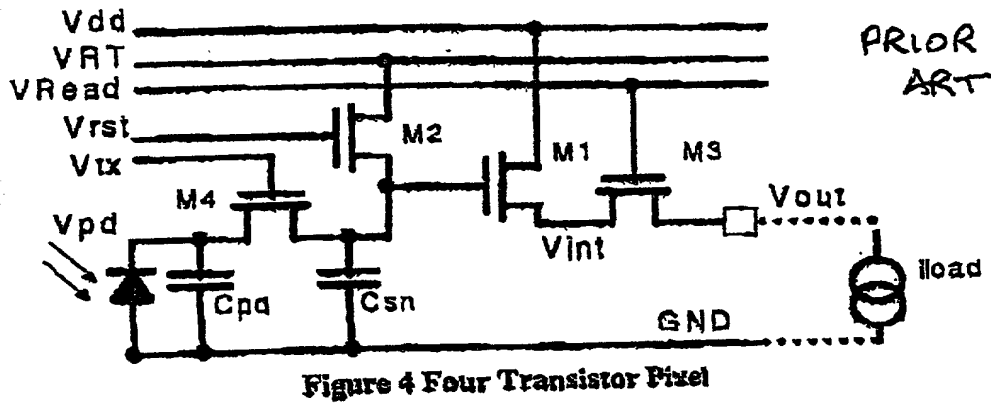


Figure 5 Sophisticated Linear Array

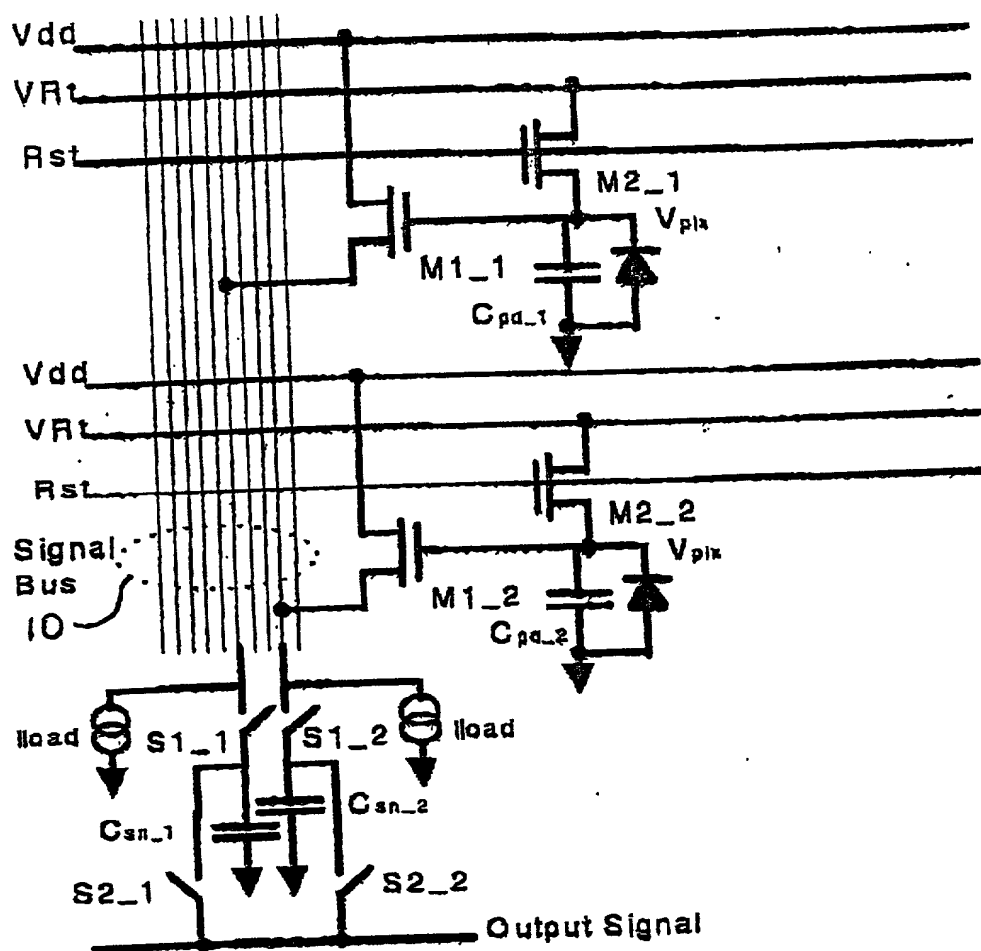


Figure 6 (Part of) New Column Structure

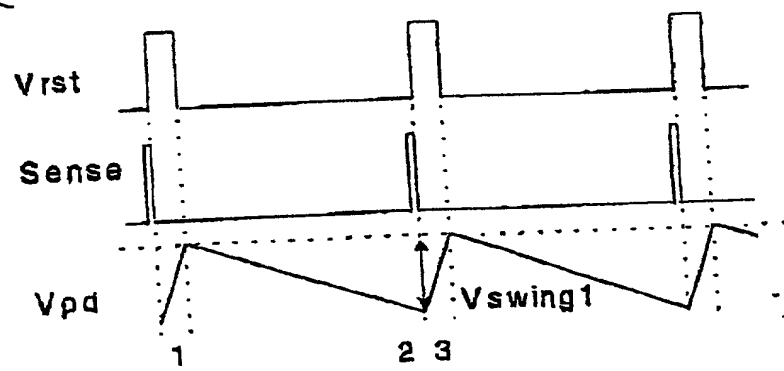


Figure 7 Timing Diagram

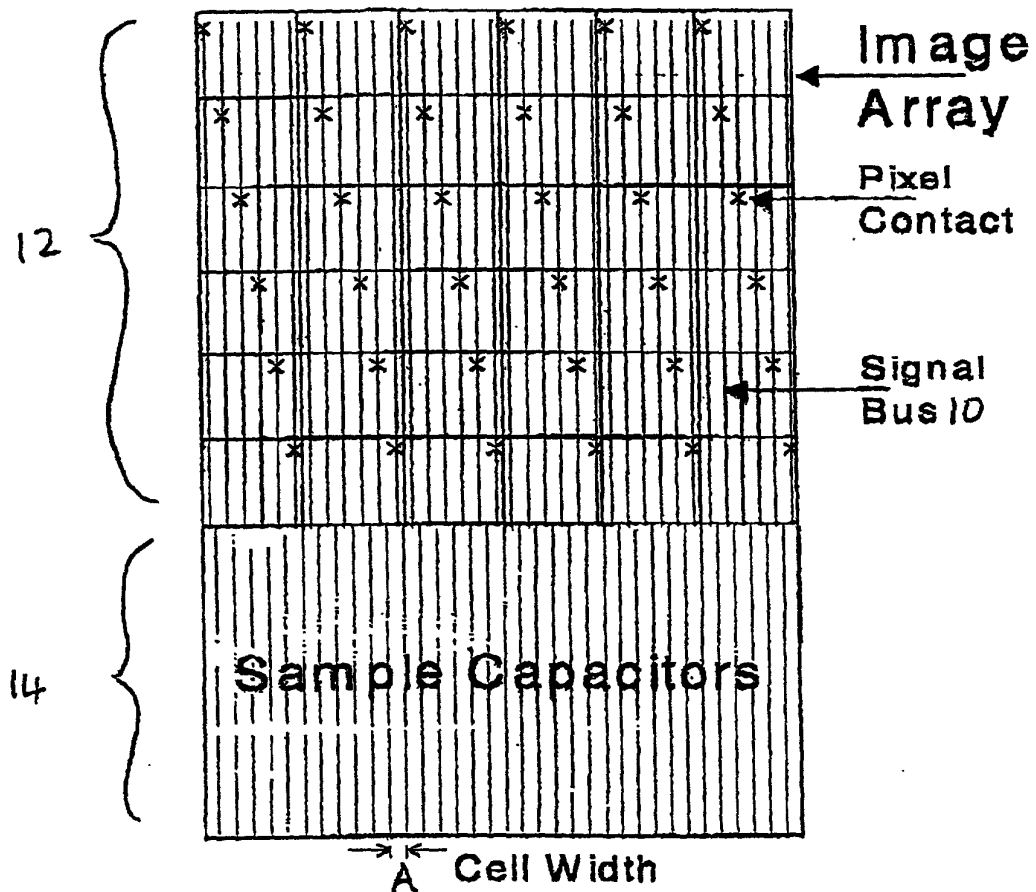


Figure 8 Typical System Layout

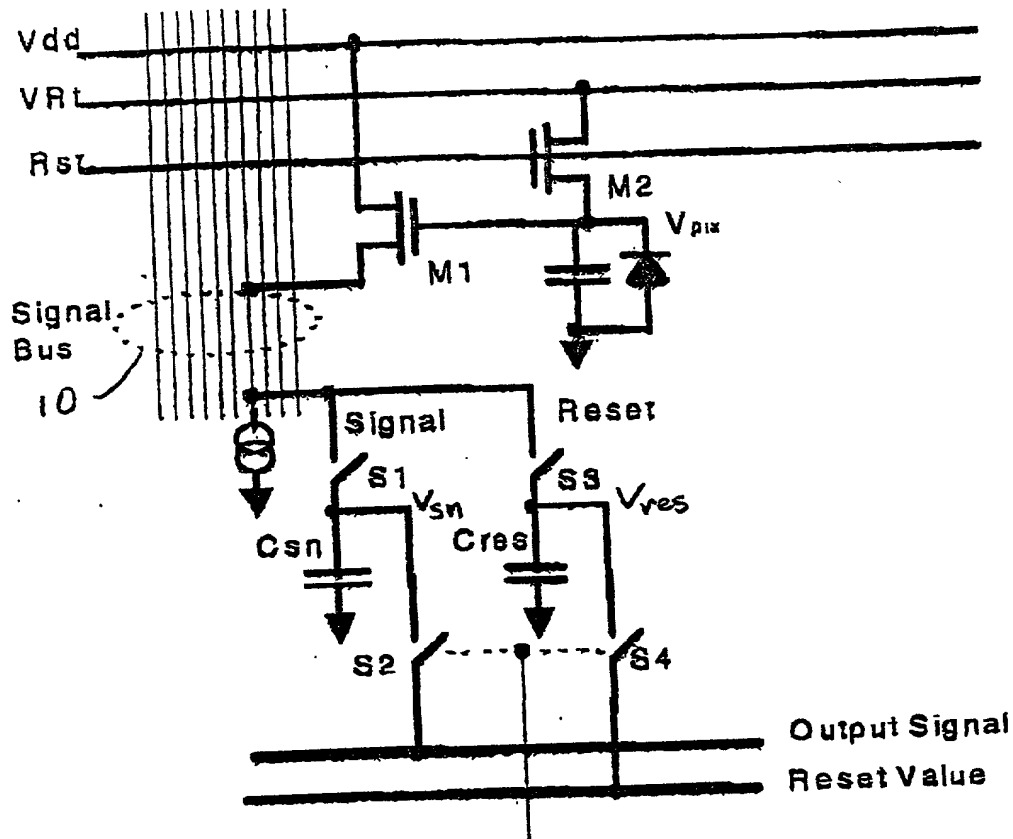


Figure 9 Improved Circuit - Offset Cancellation

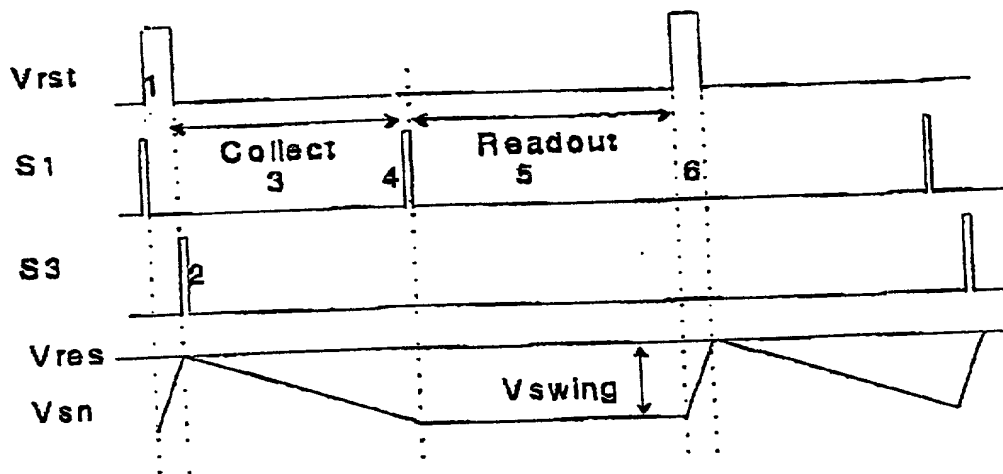


Figure 10 Offset Cancellation - Timing diagram

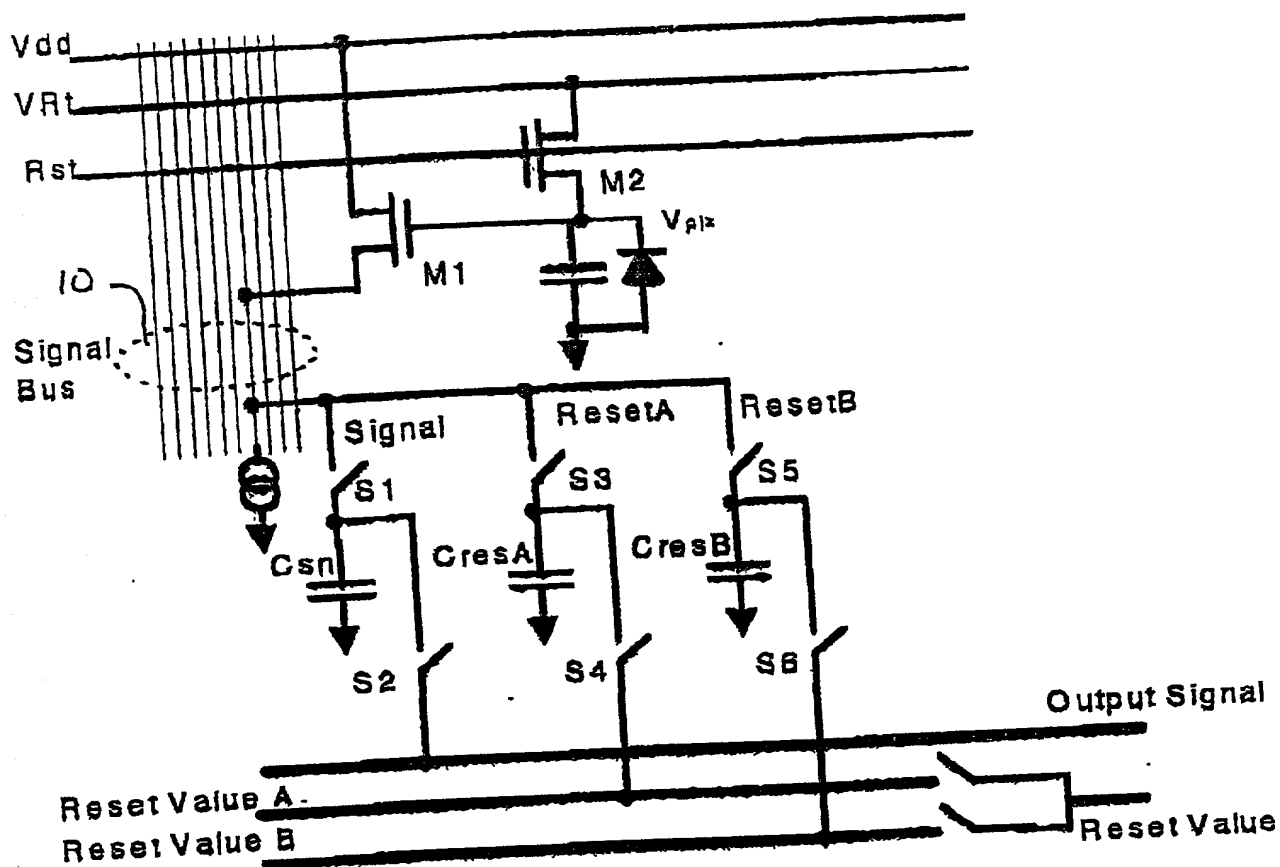


Figure 11 Improved Circuit - Offset Cancellation 2

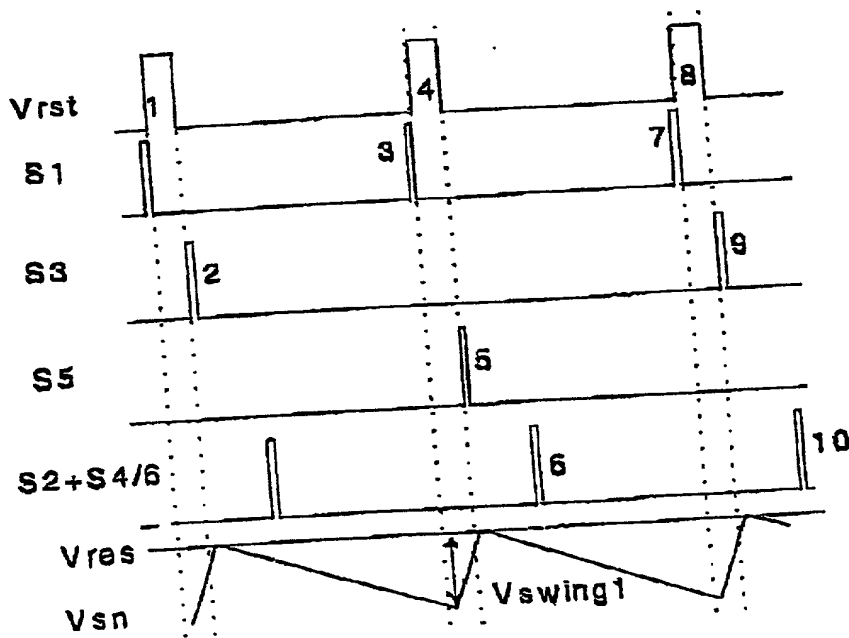


Figure 12 Offset Compensation 2 - Timing Diagram

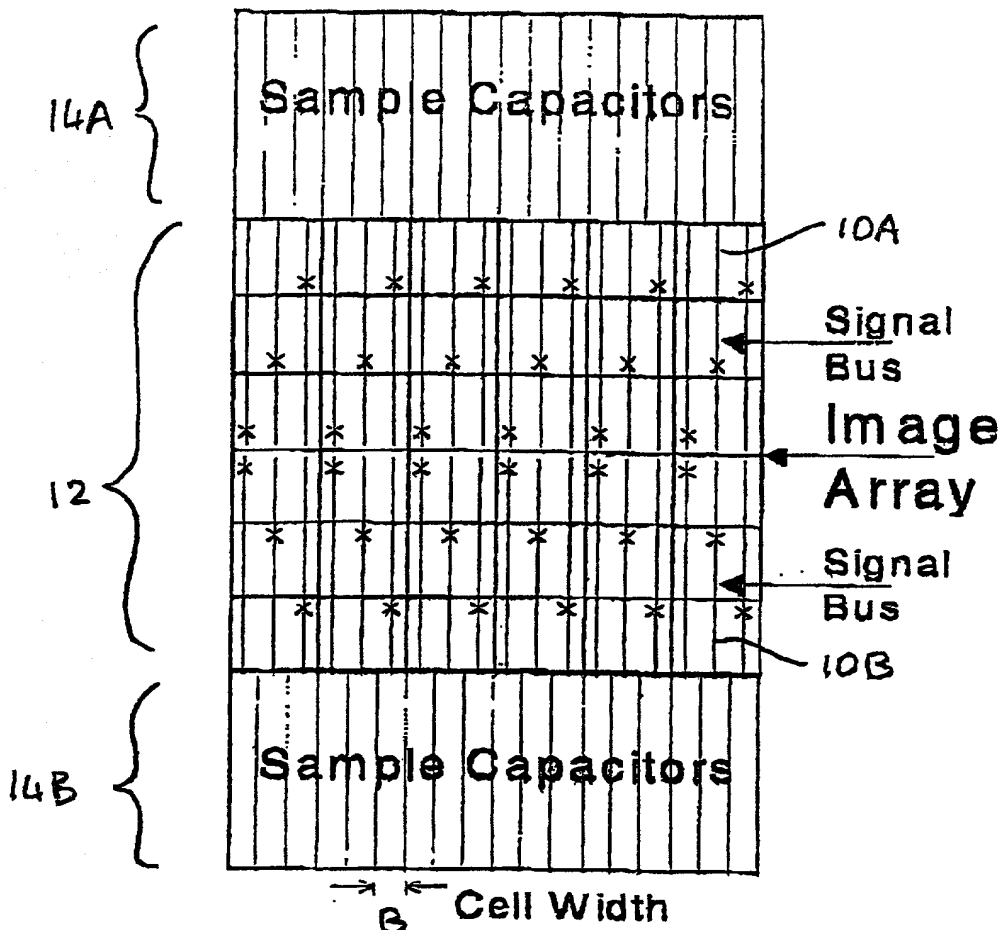


Figure 13 Improved Layout Technique

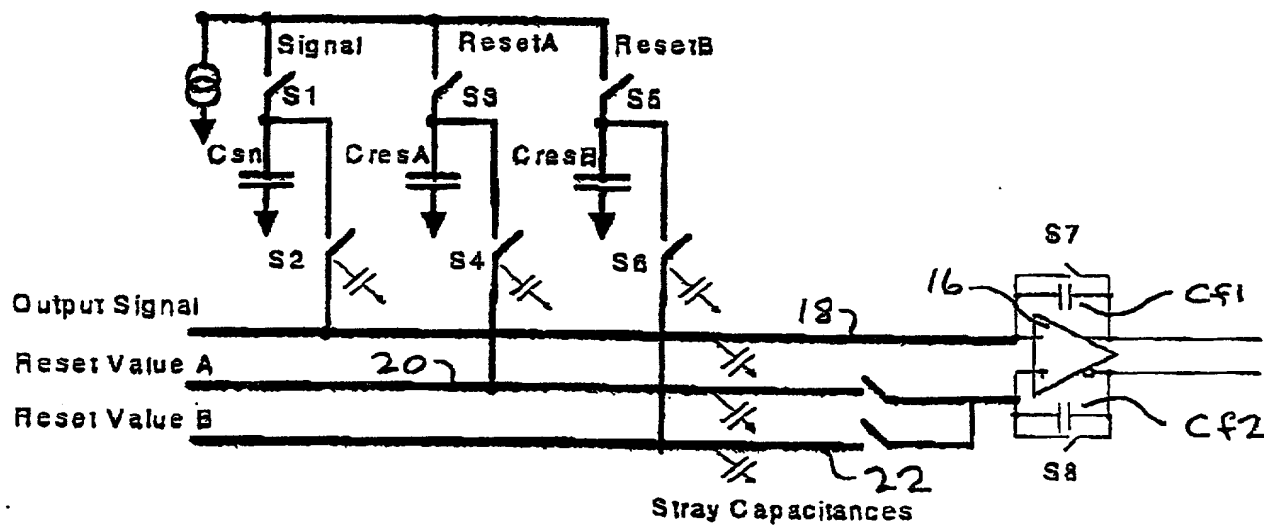


Figure 14 Preferred Readout Amplification